C355 Credit HW # 3 (Due 08/11 10 PM)  
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Q1 - Chris Kasper

Refer to the single cycle CPU diagram supplied. For the following instruction , fill up the entries in the spreadsheet supplied in class. **Instruction: slt $t0, $s1, $s2**

Given: Initially $s1=5 and $s2 = 10   
(instruction address was assumed to be location 0)

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | 0 | **K** | X |
| **Instruction[31-0]** | 0,17,18,8,0,42 | **L** | 4 |
| **Instruction[31-26] Op** | 0 | **M** | X |
| **Instruction[25-0] jimm** | X | **N** | 4 |
| **Instruction[25-21] rs** | 17 | **P** | 4 |
| **Instruction[20-16] rt** | 18 | **Q** | X |
| **Instruction[15-11] rd** | 8 | **R** | 0 |
| **Instruction[15-0] imm** | X | **RegDst** | 1 |
| **Instruction[5-0] funct** | 42 | **Jump** | 0 |
| **B** | 8 | **Branch** | 0 |
| **C** | 5 | **Zero** | 0 |
| **D** | 10 | **MemRead** | 0 |
| **E** | X | **MemtoReg** | 0 |
| **F** | 10 | **ALUop** | 10 |
| **Operation** | 0111 | **MemWrite** | 0 |
| **G** | 1 | **ALUSrc** | 0 |
| **H** | X | **RegWrite** | 1 |
| **J** | 1 | **-----------** | ----------- |

Q2 - Dallas Foglia

Assume that the single cycle CPU is executing the instruction word 0x1253FFF8 located at address 3000(decimal). The register contents before fetching the instruction were as follows:

$s1 = 60 , $s2 = 80, $s3 = 80, $s4 =100 (all decimal).

Answer the following questions:

Is any register written as a result of executing the instruction and, if so, which one?

-The BEQ instruction does not write to registers

Name any one component not used by this instruction

-Both the $s1 and $s4 registers are not used in this instruction

What is the value of “Operation” (in binary) ?

- 0110

Is the Zero signal asserted?

-Yes, the zero signal is asserted because both $s2 and $s3 are equal to one another. Additionally, BEQ is one of the only instructions that makes use of the zero signal

What is the address of the next instruction to be executed?

- 2992. Address in instruction is FFF8, which is -8.

Q3 - Alfonzo DeSantis

In the single cycle CPU the following are the latencies for different components:

Instruction Memory: 500 ps

ADD: 100 ps

MUX 20 ps

ShiftLeft2 5 ps

Registers 300 ps

Control 150 ps

Sign Extend 30 ps

ALU Control 40 ps

ALU 160 ps

Data Memory 400 ps

1. Do a componentwise analysis and determine the times at which the following signals are generated for a lw instruction assuming signal A is available at t=0. Use the provided single cycle CPU circuit diagram if necessary. (3)

L t = 100 ps

Instruction[31-0] t = 500 ps

Control signals t = 650 ps

B t = 520 ps

C/D t = 800 ps

E t = 530 ps

F t = 820 ps

G t = 980 ps

H t = 1380 ps

J t = 1400 ps

What is the slack available for asserting RegWrite? (1)

control signals @ t = 650 ps, J @ t = 1400 ps,

The slack available for RegWrite is 1400 ps - 650 ps = 750 ps

Q4 - Dallas Foglia

In the single cycle design, determine which instructions will execute correctly despite

the following faults, each considered separately. Give detailed justification (Consider

R-format,lw,sw,beq and j) (3)

* ALUOp1 stuck at 0

If the ALUOp is stuck at 0 only LW, SW, and BEQ can be performed, as the Opcodes for all other operations require ALUOp1 to be set to ‘1’.

* RegDst stuck at ‘1’

RegDst (Register Destination), is used when rewriting to a register under the following operations: Add, Sub, And, Or, SLT. If this value was locked at ‘1’ LW, SW, and BEQ would be the only instructions affected. SW and BEQ are not suppose to write registers at all, and would most likely stop working entirely. I suspect the same would happen for LW.

* MemRead stuck at ‘1’

MemRead is only used in the LW instruction. When it is stuck at value ‘1’, whatever is stored in the Data Memory will be read continuously.